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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/829,186	04/22/2004	Simon C. Steely JR.	200310150-1	6058

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EXAMINER

KIM, DANIEL Y

ART UNIT PAPER NUMBER

2185

DATE MAILED: 10/10/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

**Office Action Summary**

Application No.

10/829,186

Applicant(s)

STEELY, SIMON C.

Examiner

Daniel Kim

Art Unit

2185

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 19 July 2006.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-26 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-26 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 22 April 2004 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- |   |   |
|---|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)         | 4) <input type="checkbox"/> Interview Summary (PTO-413)           |
| 2) <input type="checkbox"/> Notice of Draftperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____                                      |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)         | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| Paper No(s)/Mail Date _____   | 6) <input type="checkbox"/> Other: _____                          |

## **DETAILED ACTION**

### ***Response to Amendment***

1. This Office Action is in response to applicant's communication filed July 19, 2006 in response to the PTO Office Action mailed May 5, 2006. The applicant's remarks and amendments to the claims and/or the specification were considered with the results that follow.

2. In response to the last Office Action, claims 1, 5, 10-11, 17 and 22 have been amended, No claims have been added or cancelled. Claims 1-26 remain pending in this application.

3. The objection to claims 5 and 11 have been withdrawn due to the amendment filed July 19, 2006.

### ***Response to Arguments***

4. Applicant's arguments with respect to claims 1-26 have been considered but are moot in view of the new ground(s) of rejection.

### ***Claim Rejections - 35 USC § 103***

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

6. Claim 1 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hagersten et al (US Patent No. 5,778,427) and Trull (US Patent No. 5,497,477).

For claim 1, Hagersten discloses a method for storing replacement data in a multi-way associative cache comprising at least one cache set (a multi-way cache of a computer system... the cache is organized using cache lines, and includes a plurality of cache lines divided into a number of segments corresponding to the number of ways, col. 3, lines 27-34), and

logically dividing the cache's cache sets into segments of at least one cache way (col. 3, lines 27-34).

Hagersten fails to disclose a method for storing replacement data, searching a cache set in accordance with a segment search sequence for a segment currently comprising a way which has not yet been accessed during a current cycle of the segment search sequence, searching the current segment in accordance with a way search sequence for a way which has not yet been accessed during a current way search cycle, or storing the replacement data in a first way which has not yet been accessed during a current cycle of the way search sequence.

Trull, however, helps disclose a cache insertion selector for accurately determining which entries of a cache are being frequently used, where the cache insertion selector monitors the access history of a slot, wherein a slot is marked as used recently when it is accessed; when a new entry is to be inserted into the cache when all

slots contain valid entries, the cache insertion selector attempts to select a slot which is not marked as used recently, and if there is no such slot, the cache insertion selector marks all slots as not used recently, and then selects one such slot (col. 2, lines 12-20).

It would have been obvious to a person of ordinary skill in the art at the time of the invention to combine Hagersten and Trull to include searching for a way or ways that have not been accessed because the cache contains a relatively small amount of memory, fills up quickly, and therefore copying an entry to the cache generally requires replacing another entry, and to help maximize performance, entries which are not being frequently used should be selected for replacement (col. 1, lines 27-32), as taught by Trull.

7. Claims 2-26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hagersten et al (US Patent No. 5,778,427), Trull (US Patent No. 5,497,477) and Rowlands et al (US Patent No. 6,748,492).

For claim 2, the combined teachings of Hagersten and Trull as per rejection of claim 1 fail to disclose a next sequential segment of the segment search sequence is considered when a segment currently being considered to receive replacement data is determined to not contain a way which has not yet been accessed during the current segment search cycle.

Rowlands helps disclose a replacement circuit that changes state for each access of a cache, irrespective of whether or not the access hits or misses (col. 14,

lines 34-36), wherein a next consecutive way is selected as the selected way, and steps are repeated for the selected index and selected way (col. 17, lines 32-35).

It would have been obvious to a person of ordinary skill in the art at the time of the invention to combine Hagersten, Trull and Rowlands to include searching a next sequential segment because this would help ensure all ways of the selected index and all indexes have been processed (col. 17, lines 36-38), as taught by Rowlands.

For claim 3, the combined teachings of Hagersten, Trull and Rowlands as per rejection of claim 2 further help disclose a next sequential way of the way search sequence is considered when a way currently being considered to receive replacement data is determined to have been accessed during the current way search cycle (Rowlands: col. 17, lines 32-25).

For claim 4, the combined teachings of Hagersten, Trull and Rowlands as per rejection of claim 2 further help disclose considering a current segment for storing replacement data until all ways in the current segment have been accessed during the current way search cycle (Rowlands: col. 17, lines 32-35); and selecting for replacement consideration a next sequential segment in the segment search sequence (Rowlands: col. 17, lines 32-35).

For claim 5, the combined teachings of Hagersten, Trull and Rowlands as per rejection of claim 2 further help disclose repeating the considering and selecting for each segment in the segment search sequence (Rowlands: col. 17, lines 32-35).

For claim 6, the combined teachings of Hagersten, Trull and Rowlands as per rejection of claim 2 further help disclose repeating the segment search sequence when

all segments of the cache set are determined to comprise ways which have been accessed during the current segment search cycle (Rowlands: col. 14, lines 34-36; col. 17, lines 32-25).

For claim 7, the combined teachings of Hagersten, Trull and Rowlands as per rejection of claim 2 further help disclose searching way access indicators corresponding to ways of the current segment, wherein each way access indicator indicates whether a corresponding way has been accessed during a current way search cycle (Trull: col. 2, lines 12-20; Rowlands: if a least recently used policy is employed, the LRU policy for the index identified may be set to indicate that the way identified is least recently used, col. 6, line 67, col. 7, lines 1-3).

For claim 8, the combined teachings of Hagersten, Trull and Rowlands as per rejection of claim 7 further help disclose setting the way access indicators corresponding to the current segment's ways to a value indicating the ways have not been accessed (col. 2, lines 12-20).

For claim 9, the combined teachings of Hagersten, Trull and Rowlands as per rejection of claim 7 further help disclose prior to the searching of the cache set, determining whether a way of the cache set contains invalidated data, and storing the replacement data in the way containing the invalidated data (Rowlands: transactions may include various coherency commands such as an invalidate command which may or may not involve a transfer of data, col. 4, lines 40-42; if a transaction is a miss in a cache, the cache may select a way for eviction to receive a line fill of the missing line; more particularly, the replacement circuit may be configured to select the way to be

evicted, which may be provided as the way selection, and the valid bit in the evicted entry may be cleared to invalidate the cache line, col. 9, lines 45-50).

For claim 10, the combined teachings of Hagersten, Trull and Rowlands as per rejection of claim 9 are incorporated herein.

These teachings further help disclose a method for managing a multi-associative cache comprising at least one cache set, the method comprising:

logically dividing each cache set of the cache into segments each comprising at least one cache way (Hagersten: col. 3, lines 27-34);

storing replacement data in an invalidated way, if any, in the cache set, in response to a cache miss, and setting, in response to a processor accessing the replacement data, a way access indicator corresponding to the accessed way to a value indicating the way has been accessed (Rowlands: col. 4, lines 40-42; col. 9, lines 45-50; Trull: col. 2, lines 12-20); and

selecting, when no invalidated way is in the cache set, a current segment of a segment search sequence for an available way; and searching the current segment in accordance with a way search sequence, for a next way not yet accessed during a current cycle of the way search sequence (Rowlands: col. 4, lines 40-42; col. 9, lines 45-50; Trull: col. 2, lines 12-20).

For claim 11, the combined teachings of Hagersten, Trull and Rowlands as per rejection of claim 10 further help disclose when a way not yet accessed during a current cycle of the way search sequence is located, storing replacement data in the located way (Rowlands: col. 4, lines 40-42; col. 9, lines 45-50; Trull: col. 2, lines 12-20).



For claim 12, the combined teachings of Hagersten, Trull and Rowlands as per rejection of claim 11 further help disclose providing access to the way containing the replacement data (Rowlands: a direct access transaction specifies a cache storage entry to be accessed in response to the transaction; the cache may access the cache storage entry and either read the data from the cache entry or write data from the transaction to the storage entry, col. 2, lines 34-41).

For claim 13, the combined teachings of Hagersten, Trull and Rowlands as per rejection of claim 12 further help disclose setting a way access indicator corresponding to the accessed way to a value indicating the way has been accessed (Trull: col. 2, lines 12-20).

For claim 14, the combined teachings of Hagersten, Trull and Rowlands as per rejection of claim 10 further help disclose when a way not yet accessed during a current cycle of the way search sequence is not located, setting way access indicators corresponding to all ways in the current segment to a value indicating the ways are available (Trull: col. 2, lines 12-20).

For claim 15, the combined teachings of Hagersten, Trull and Rowlands as per rejection of claim 14 further help disclose selecting a next segment in the segment search sequence as the current segment and repeating the segment search cycle (Rowlands: col. 17, lines 32-35).

For claim 16, the combined teachings of Hagersten, Trull and Rowlands as per rejection of claim 10 further help disclose providing, in response to a cache hit, access to the way containing the requested data and setting a way access indicator

corresponding to the accessed way to a value indicating the way was accessed (Trull: col. 2, lines 12-20).

For claim 17, the combined teachings of Hagersten, Trull and Rowlands as per rejection of claim 10 are incorporated herein.

These teachings further help disclose a processing environment comprising:

a processor (Hagersten: a multi-way cache of a computer system having a main memory and one or more processors, abstract);

a multi-way associative cache comprising at least one cache set (Hagersten: col. 3, lines 27-34);

a cache controller configured to logically divide the cache's sets into segments of at least one cache way (Hagersten: a cache manager, col. 3, line 24; col. 3, lines 27-34), and comprising replacement logic that, in response to a cache miss, stores the replacement data in a way, if available, that contains invalidated data, and if not available, searches a cache set in accordance with a segment search sequence for a segment comprising a way which has not yet been accessed during a current cycle of the segment search sequence, and searches each segment in accordance with a way search sequence for a way which has not yet been accessed during a current way search cycle; and stores the replacement data in a first way which has not yet been accessed during a current cycle of the way search sequence (Rowlands: col. 14, lines 34-36; col. 4, lines 40-42; col. 9, lines 45-50; col. 6, line 67, col. 7, lines 1-3; Trull: col. 2, lines 12-20).

For claim 18, the combined teachings of Hagersten, Trull and Rowlands as per rejection of claim 17 further help disclose replacement logic considers a next sequential segment of the segment search sequence when a segment currently being considered to receive replacement data is determined to not contain a way which has not yet been accessed during the current segment search cycle (Rowlands: col. 17, lines 32-25).

For claim 19, the combined teachings of Hagersten, Trull and Rowlands as per rejection of claim 17 further help disclose the replacement logic considers a next sequential way of the way search sequence when a way currently being considered to receive replacement data is determined to have been accessed during the current way search cycle (Rowlands: col. 17, lines 32-25).

For claim 20, the combined teachings of Hagersten, Trull and Rowlands as per rejection of claim 17 further help disclose the replacement logic considers a current segment for storing replacement data and selects for replacement consideration a next sequential segment in the segment search sequence when all ways in the current segment have been accessed during the current way search cycle (Rowlands: col. 17, lines 32-25; Trull: col. 2, lines 12-20).

For claim 21, the combined teachings of Hagersten, Trull and Rowlands as per rejection of claim 20 further help disclose the replacement logic searches way access indicators corresponding to ways of the current segment, wherein each way access indicator indicates whether a corresponding way has been accessed during a current way search cycle (Trull: col. 2, lines 12-20; Rowlands : col. 6, line 67, col. 7, lines 1-3).

For claim 22, the combined teachings of Hagersten, Trull and Rowlands as per rejection of claim 17 are incorporated herein.

These teachings further help disclose a processing environment comprising:  
means for logically dividing at least one cache set of a multi-way associative cache into segments of at least one cache way (Hagersten: abstract; col. 3, lines 27-34; col. 3, line 24; col. 3, lines 27-34); and

means for storing, in response to a cache miss, replacement data in a way, if available, that contains invalidated data, and if not available, searches a cache set in accordance with a segment search sequence for a segment comprising a way which has not yet been accessed during a current cycle of the segment search sequence, and searches each segment in accordance with a way search sequence for a way which has not yet been accessed during a current way search cycle; and stores the replacement data in a first way which has not yet been accessed during a current cycle of the way search sequence (Rowlands: col. 14, lines 34-36; col. 4, lines 40-42; col. 9, lines 45-50; col. 6, line 67, col. 7, lines 1-3; Trull: col. 2, lines 12-20).

For claim 23, the combined teachings of Hagersten, Trull and Rowlands as per rejection of claim 22 further help disclose the means for storing considers a next sequential segment of the segment search sequence when a segment currently being considered to receive replacement data is determined to not contain a way which has not yet been accessed during the current segment search cycle (Rowlands: col. 17, lines 32-25).

For claim 24, the combined teachings of Hagersten, Trull and Rowlands as per rejection of claim 22 further help disclose the means for storing considers a next sequential way of the way search sequence when a way currently being considered to receive replacement data is determined to have been accessed during the current way search cycle (Rowlands: col. 17, lines 32-25).

For claim 25, the combined teachings of Hagersten, Trull and Rowlands as per rejection of claim 22 further help disclose the means for storing considers a current segment for storing replacement data and selects for replacement consideration a next sequential segment in the segment search sequence when all ways in the current segment have been accessed during the current way search cycle (Trull: col. 2, lines 12-20; Rowlands : col. 6, line 67, col. 7, lines 1-3).

For claim 26, the combined teachings of Hagersten, Trull and Rowlands as per rejection of claim 22 further help disclose the means for storing searches way access indicators corresponding to ways of the current segment, wherein each way access indicator indicates whether a corresponding way has been accessed during a current way search cycle (Trull: col. 2, lines 12-20; Rowlands : col. 6, line 67, col. 7, lines 1-3).

***Citation of Pertinent Prior Art***

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Coyle et al (US Patent No. 5,367,653) discloses a reconfigurable set associative cache memory including partitioning for the highest number of ways in a multi-way associative cache.

York (US Patent No. 6,745,291) discloses an n-way set associative data cache system comprises a cache controller adapted to receive a request for data and instructions, and page tags used for comparison with page entry addresses in directories.

#### ***Contact Information***

9. Any inquiries concerning this action or earlier actions from the examiner should be directed to Daniel Kim, reachable at 571-272-2742, on Mon-Fri from 10:00am-6:30pm. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sanjiv Shah, is also reachable at 571-272-4098.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information from published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. All questions regarding access to the Private PAIR system should be directed to the Electronic Business Center (EBC), reachable at 866-217-9197.

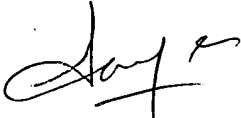
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